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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,570	04/01/2004	Nicholas Carl Seroff	STL11398	9404
7590 David K. Lucente Seagate Technology LLC Intellectual Property - COL2LGL 389 Disc Drive Longmont, CO 80503			EXAMINER CONTINO, PAUL F	
			ART UNIT 2114	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE			MAIL DATE	DELIVERY MODE
3 MONTHS			01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/815,570

Applicant(s)

SEROFF, NICHOLAS CARL

Examiner

Paul Contino

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 April 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION: Non-Final Rejection

Drawings

1. The drawings are objected to because Figure 7 shows an element “TEM” which should read “ETM”. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Byrne et al. (U.S. Patent No. 7,007,201).

As in claim 1, Byrne et al. discloses an integrated circuit device, comprising:

a controller (*Fig. 2 #12A; column 2 lines 25-29*); and

a serial trace port (*Fig. 2 #14/108; column 3 lines 32-43; column 5 lines 62-64; ETM 14 is interpreted as a serial trace port*), wherein the serial trace port provides controller trace data and wherein the controller trace data is provided external to the integrated circuit device using a differential serial channel (*Fig. 2 column 3 lines 34-36, where the output on 108 is interpreted as a differential serial channel*).

As in claim 3, Byrne et al. discloses a second controller, wherein the serial trace port also provides controller trace data of the second controller (*Fig. 2 #12B; column 3 lines 34-36, where the selected processor 12 may be processor 12A or 12B*).

As in claim 4, Byrne et al. discloses the serial trace port receives a reference clock signal and provides a clock signal to each of the controller and second controller (*Fig. 2 #104; column 3 lines 4-5, TCK; it is interpreted that the entire interface containing all inputs and outputs 104, 106, 108 is considered a serial trace port*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2, 5, 6, 8, 9, 10, 11, 13, 14, 15, 16, 17, 19, 20, 21, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne et al. in view of NS (*SCAN921023 and SCAN921224 20-66 MHz 10 Bit But LVDS*).

As in claim 2, Byrne et al. teaches of a differential serial channel. However, Byrne et al. fails to teach of transmitting data, control and timing information in a serial stream. NS teaches of transmitting data, control and timing information in a serial stream (*page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose*

serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the serial component transmission as taught by NS in the invention of Byrne et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which serial data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 5, Byrne et al. teaches of a trace buffer operatively coupled to the controller and the second controller (*Fig. 2 #14; column 1 lines 15-22, where the ETM is interpreted as a trace buffer*). However, Byrne et al. fails to teach of a serializer. NS teaches of a serializer, operatively coupled between the differential serial channel and the trace buffer, which converts a parallel data stream from the trace buffer to a serial data stream for the differential serial channel (*page 1*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the differential transmitter as taught by NS in the invention of Byrne et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 6, Byrne et al. teaches of a trace buffer operatively coupled to the controller and the second controller (*Fig. 2 #14; column 1 lines 15-22, where the ETM is interpreted as a trace buffer*). However, Byrne et al. fails to teach of a serializer. NS teaches of a serializer, operatively coupled between the differential serial channel and the trace buffer, which converts a parallel data stream from the trace buffer to a serial data stream for the differential serial channel (*page 1*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the differential transmitter as taught by NS in the invention of Byrne et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 8, the combined invention of Byrne et al. and NS teaches the serial trace port also provides a serializer clock signal to the serializer (*Byrne et al.: Figure 2, column 3 lines 4-5, TCK; NS: page 2; where it is interpreted that the TCK as taught in Byrne et al. provides the TCLK as taught by NS*).

As in claim 9, Byrne et al. teaches of a test apparatus, comprising:
an electronic device comprising a plurality of controllers (*Fig. 2 #12A,B; column 2 lines 25-29*), a trace buffer operatively coupled to the plurality of controllers (*Fig. 2 #14; column 1 lines 15-22, where the ETM is interpreted as a trace buffer*); and

a workstation, operatively coupled to the electronic device, for communicating with the electronic device (*column 1 lines 20-21, external trace port analyzer*).

However, Byrne et al. fails to teach of a differential transmitter. NS teaches of a differential transmitter (*page 1*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the differential transmitter as taught by NS in the invention of Byrne et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 10, the combined invention of Byrne et al. and NS teaches of a serializer, operatively coupled between the differential transmitter and the trace buffer, which converts a parallel data stream from the trace buffer to a serial data stream for the differential transmitter (*NS: page 1*).

As in claim 11, the combined invention of Byrne et al. and NS teaches of a clock means for providing clock signals to each of the plurality of controllers (*Byrne et al.: Fig. 2; column 3 lines 4-5, TCK*) and the serializer (*NS: page 2, TCLK*).

As in claim 13, the combined invention of Byrne et al. and NS teaches of a converter operatively coupled between the electronic device and the workstation for converting data

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received from the electronic device to a parallel data stream for use by the workstation (*Byrne et al.: column 1 lines 20-22, external trace port analyzer; NS: page 2 figure, right side*).

As in claim 14, the combined invention of Byrne et al. and NS teaches of transmitting data, control and timing information in a serial stream (*NS: page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits*).

As in claim 15, the combined invention of Byrne et al. and NS teaches the converter relays test commands from the workstation to the electronic device (*Byrne et al.: Fig. 2; column 1 lines 20-22 and column 2 lines 37-67, where it is interpreted that the converter includes the JTAG interface and couples the JTAG device, which receives test commands from the analyzer workstation, along with the converted data stream, to the analyzer workstation*).

As in claim 16, the combined invention of Byrne et al. and NS teaches of transmitting data, control and timing information in a serial stream (*NS: page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits*).

As in claim 17, Byrne et al. teaches of a method of transforming trace data from a plurality of embedded controllers of an electronic device (*Fig. 2 #12A,B; column 2 lines 25-29*), comprising the steps of:

storing trace data from each of the embedded controllers in memory (*Fig. 2 #14; column 1 lines 15-22, where the ETM FIFO is interpreted as memory*);

retrieving the trace data from the memory and retrieving the trace data as a serial stream (*column 1 lines 55-56 and column 5 lines 62-64*); and

transmitting the serial stream using at least one transmitter (*column 1 lines 19-22*).

However, Byrne fails to teach of serialization or differential transmission. NS teaches of converting data to a serial stream and transmitting the serial stream using at least one differential transmitter (*page 1*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the serialization and differential transmitter as taught by NS in the invention of Byrne et al. This would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems.

As in claim 19, the combined invention of Byrne et al. and NS teaches of receiving the transmitted serial stream and converting the received serial stream into a parallel stream (*NS: page 2 figure, right side*); and

displaying at least a portion of the parallel stream as controller trace data (*Byrne et al.: column 1 lines 20-22, where it is interpreted that the transmitted trace data is being “displayed” to an analyzer after deserialization*).

As in claim 20, the combined invention of Byrne et al. and NS teaches of transmitting a second serial stream using a second differential transmitter (*Byrne et al.: column 5 lines 19-25; NS: page 1; where an ETM dedicated to a single processor would necessarily use a respective differential transmitter*).

As in claim 21, the combined invention of Byrne et al. and NS teaches the serial stream contains trace data of a first controller of the plurality of embedded controllers and the second serial stream contains trace data of a second controller of the plurality of embedded controllers (*Byrne et al.: column 5 lines 19-25; NS: page 1; where an ETM dedicated to a single processor would necessarily use a respective differential transmitter containing data of the respective processor*).

As in claim 22, the combined invention of Byrne et al. and NS teaches the transmitted serial stream and the second serial stream each comprise data, control and clock information (*NS: page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits*).

As in claim 23, the combined invention of Byrne et al. and NS teaches of transmitting data, control and timing information in a serial stream (*NS: page 2, figure including Frame, Control, and Data, where the first and third paragraphs under Data Transfer disclose serialization of the Frame/Control/Data from DIN0-DIN9 and transmission over a differential channel along with clock bits*).

* * *

4. Claims 7, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrne et al. in view of NS, further in view of Agarwala et al. (U.S. PGPub 2006/0288254).

As in claim 7, the combined invention of Byrne et al. and NS teaches of a parallel data stream. However, the combined invention of Byrne et al. and NS fails to teach of compressing data. Agarwala et al. teaches of a parallel data stream comprising compressed data (*Fig. 4,8,9; paragraphs [0043] and [0059]-[0066]*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the data compression as taught by Agarwala et al. in the combined invention of Byrne et al. and NS. This would have been obvious because compression of data as taught by Agarwala et al. allows for faster transmission of data and conservation of inter/extra-circuit communication bandwidth.

As in claim 12, the combined invention of Byrne et al. and NS teaches of a parallel data stream. However, the combined invention of Byrne et al. and NS fails to teach of compressing data. Agarwala et al. teaches of a parallel data stream comprising compressed data (*Fig. 4,8,9; paragraphs [0043] and [0059]-[0066]*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the data compression as taught by Agarwala et al. in the combined invention of Byrne et al. and NS. This would have been obvious because compression of data as taught by Agarwala et al. allows for faster transmission of data and conservation of inter/extra-circuit communication bandwidth.

As in claim 18, the combined invention of Byrne et al. and NS teaches of converting retrieved trace data into a serial stream. However, the combined invention of Byrne et al. and NS fails to teach of compressing data. Agarwala et al. teaches of a data stream comprising compressed data before transmission (*Fig. 4,8,9; paragraphs [0043] and [0059]-[0066]*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the data compression as taught by Agarwala et al. in the combined invention of Byrne et al. and NS. This would have been obvious because compression of data as taught by Agarwala et al. allows for faster transmission of data and conservation of inter/extra-circuit communication bandwidth.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 5,764,885 Sites et al. discloses multiple processors being traced.

U.S. Patent No. 6,973,592 Debling discloses multiple serial outputs and processors.

U.S. Patent No. 5,165,036 Miyata et al. discloses multiple controllers being traced.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER